EXHIBIT M

Analysis of Infringement of U.S. Patent No. 7,080,330 by MediaTek Inc. and MediaTek USA Inc.
(Based on Public Information Only)

Plaintiff Ocean Semiconductor LLC ("Ocean Semiconductor"), provides this preliminary and exemplary infringement analysis with respect to infringement of U.S. Patent No. 7,080,330, entitled "CONCURRENT MEASUREMENT OF CRITICAL DIMENSION AND OVERLAY IN SEMICONDUCTOR MANUFACTURING" (the "'330 patent) by MediaTek Inc. and MediaTek USA Inc. ("MediaTek"). The following chart illustrates an exemplary analysis regarding infringement by Defendant MediaTek semiconductor products, systems, devices, components, integrated circuits, and products containing such circuits, fabricated or manufactured using ASML's semiconductor fabrication or manufacturing equipment and/or platforms (e.g., ASML's YieldStar system). Such products include, without limitation, mobile devices (e.g., Helio G, Helio A, Helio P, Helio X, mid-range 4G devices, and Google Mobile Services express devices), tablet products (e.g., MiraVision), internet of things devices (e.g., i500, i350, i300A, i300B, MT3620, MT2625, MT2621, MT2601, MT2523G, MT2523D, MT2511, MT6280, MT2502, MT5931, MT3332, MT 2503, MT3333, MT3303, MT3337, and MT3339), automotive devices (e.g., Autus I20 (MT2712) devices, Autus R10 (MT2706) devices, and Autus T10 (MT2635) devices), networking and broadband devices (e.g., MediaTek T750 MT7688A, MT7628K/N/A, MT7623N/A, MT7622, MT7621A/N, MT7620N/A, RT3662, RT3883, MT7688K, MT5932, MT8167S, MT7686, MT7682, MT7697H/HD, MT7681, MT7687F, MT7697, MT7697D, MT7601E, MT7601U, MT7603E, MT7603U, MT7610E, MT7610U, MT7612E, MT7612U, MT7615, MT7615B, MT7615S, MT7662E, MT7662U, MT7668, RT3062, RT3070, RT3562, RT3573, RT3593, RT5370, RT5572, RT5592, MT3729, MT7601, MT7610, MT7630, RT5372, RT539x, RT8070, RT2870, RT2890, RT309x, RT3290, RT3370, RT3572, RT2070, RT2760, RT2770, RT2790, and RT2860), and home devices (e.g., MT8516 SoM, MT8516, MT8507, MT8502, MediaTek C4X Development Kit for Amazon AVS, MT8516 2-Mic Development Kit for Amazon AVS, MT8516, MT8693, MT8685, MT8581, MT8580, MT8563, MT8553, MT1389/G, MT1389/J, MT1389/Q, S900 (MT9950), MT9613, MT9685, MT9602, MT5592, MT5582, MT5596, MT5597, MT5580, MT5561, MT5505, MT5398, MT5396, MT1959, MT1887, MT1865, MT1862, and MT1398), and similar systems, products, devices, and integrated circuits (collectively, the "'330 Infringing Instrumentalities").

The analysis set forth below is based only upon information from publicly available resources regarding the '330 Infringing Instrumentalities, as MediaTek has not yet provided any non-public information.

Unless otherwise noted, Ocean Semiconductor contends that MediaTek directly infringes the '330 patent in violation of 35 U.S.C. § 271(g) by using, selling, and/or offering to sell in the United States, and/or importing into the United States, the '330 Infringing Instrumentalities. The following exemplary analysis demonstrates that infringement. Unless otherwise noted, Ocean Semiconductor further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. § 271(b) in conjunction with other evidence of liability.

Unless otherwise noted, Ocean Semiconductor believes and contends that each element of each claim asserted herein is literally met through MediaTek provision or importation of the '330 Infringing Instrumentalities. However, to the extent that MediaTek attempts to allege that any asserted claim element is not literally met, Ocean Semiconductor believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the '330 Infringing Instrumentalities, Ocean Semiconductor did not identify any substantial differences between the elements of

the patent claims and the corresponding features of the ’330 Infringing Instrumentalities, as set forth herein. In each instance, the identified feature of the ’330 Infringing Instrumentalities performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

Ocean Semiconductor notes that the present claim chart and analysis are necessarily preliminary in that Ocean Semiconductor has not obtained substantial discovery from MediaTek nor has MediaTek disclosed any detailed analysis for its non-infringement position, if any. Further, Ocean Semiconductor does not have the benefit of claim construction or expert discovery. Ocean Semiconductor reserves the right to supplement and/or amend the positions taken in this preliminary and exemplary infringement analysis, including with respect to literal infringement and infringement under the doctrine of equivalents, if and when warranted by further information obtained by Ocean Semiconductor, including but not limited to information adduced through information exchanges between the parties, fact discovery, claim construction, expert discovery, and/or further analysis.

USP 7,080,330	Infringement by the '330 Accused Instrumentalities
19. A method for monitoring and controlling a semiconductor fabrication process comprising:	To the extent that the preamble of Claim 19 is a limitation, ASML's YieldStar system monitors and controls a semiconductor fabrication process. For example, a variety of YieldStar systems perform this method, as follows: "The YieldStar 380G offers the nanometer-level precision necessary to monitor and control processes for today's most advanced chips." *See* YieldStar380G Product Overview, *available at* https://www.asml.com/en/products/metrology-and-inspection-systems/yieldstar-380g (last visited Oct. 12, 2020). The YieldStar 375F also performs this method, as follows: "The YieldStar 375F offers the nanometer-level precision necessary to monitor and control processes for today's most advanced chips." *See* YieldStar 375F Product Overview, *available at* https://www.asml.com/en/products/metrology-and-inspection-systems/yieldstar-375f (last visited Oct. 12, 2020). The YieldStar system is further describes as follows: "The YieldStar platform offers a standalone configuration and a configuration integrated in the resist track of a litho cluster. When integrated, a rich set of data becomes available from every production lot running through the litho cluster. This allows the lithography engineer to monitor, diagnose and further optimize production performance, fine tune production sampling schemes and offload metrology from today's offline metrology tools such as CD-SEM." *See* Marlene Strobl et al., *Integrated ADI optical metrology solution for lithography process control of CD and OV*, Metrology, Inspection, and Process Control for Microlithography 28, at 1 (Apr. 2, 2014) ("Integrated ADI")
providing a plurality of wafers undergoing the fabrication process;	ASML's YieldStar system provides a plurality of wafers undergoing the fabrication process. For example, ASML's YieldStar system provides multiple wafers undergoing the fabrication process, as follows: "To estimate the repeatability errors, we have performed TMU measurements on YieldStar 5th-gen. We restrict here to measure all

targets in Set 1, together with the C16 targets in Set 2 and 3. We were able to measure down to C6 with using the YieldStar in inline operation. For C4 we have used offline overlay extraction, which will be discussed in Section 3.4. The measurements are eight repeated runs in TIS mode with in between wafer (un)load and include sensor asymmetry correction (AC3). For practical reasons we have compromised on the total measurement time by measuring only four metrology blocks per exposure field within a wafer radius of 145 mm."

See Victor Calado et al., *Study of μDBO overlay target size reduction for application broadening*, SPIE Advanced Lithography 2018, at 4 (Mar. 13, 2018) ("Overlay Study")

Additionally, the YieldStar system provides a plurality of wafers through increased wafer lot "throughput," as described below:

"The YieldStar 375F has a throughput to match the productivity of our fastest lithography systems. It can measure thousands of data points per lot and do so faster than previous solutions, reducing chipmakers' metrology costs."

See YieldStar 375F Product Overview, *available at* https://www.asml.com/en/products/metrology-and-inspection-systems/yieldstar-375f (last visited Oct. 12, 2020).

Further, the YieldStar system is shown as being integrated in a wafer manufacturing process and provides a plurality of water through such process, as shown below:

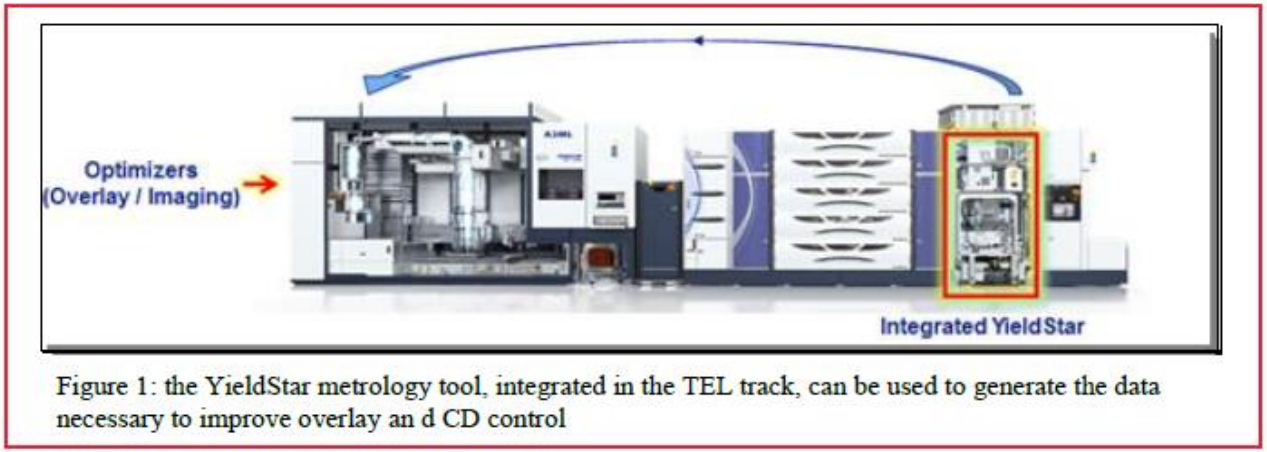
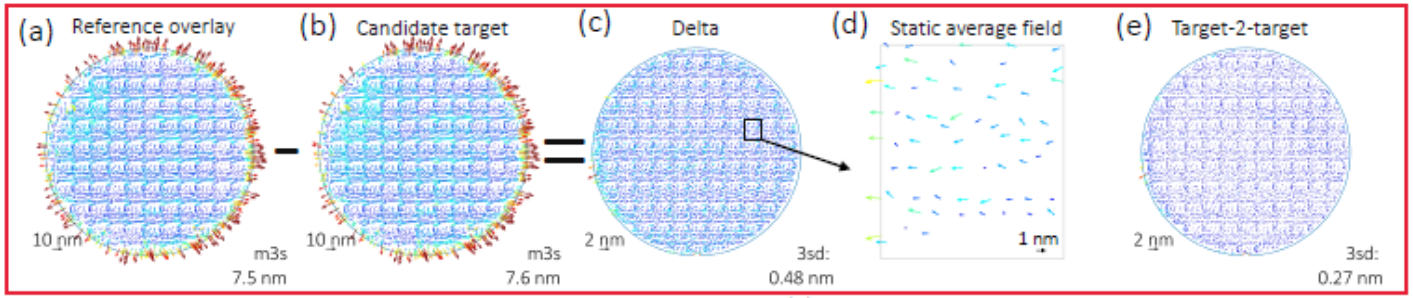


Figure 1: the YieldStar metrology tool, integrated in the TEL track, can be used to generate the data necessary to improve overlay an d CD control

	See Integrated ADI at 2.
mapping the plurality of wafers into one or more logical grids comprising one or more portions in which a grating structure for use in concurrent measurements is formed;	ASML's YieldStar system maps the plurality of wafers into one or more logical grids comprising one or more portions in which a grating structure for use in concurrent measurements is formed. The YieldStar system records dense overlay maps depicting the average overlay of three wafers, as follows:  Figure 2. Dense overlay maps recorded on a YieldStar system. (a) The overlay map of the Reference overlay. The reference here is the mean overlay of the three C16 targets. (b) The reference overlay is compared to a candidate, here C16 Set 1. (c) The difference ("Delta") between the reference and delta is shown, note the scale is now reduced to 2 nm. (d) The static average field is plotted and subsequently subtracted resulting in (e) the target-2-target delta map. *See* Overlay Study at 3. *See also id.* at 2 ("In addition, reduced sized targets have the advantage to be placed in-die (enabling intra-eld corrections) instead of in the scribe lanes only, allowing more freedom and flexibility in metrology target placement. It is also desirable to have multiple targets of different designs nearby each other to guarantee accurate overlay measurements during stack changes by allowing the freedom to choose an overlay target that matches the optical properties of the stack.") *See also id.* at Fig. 1:

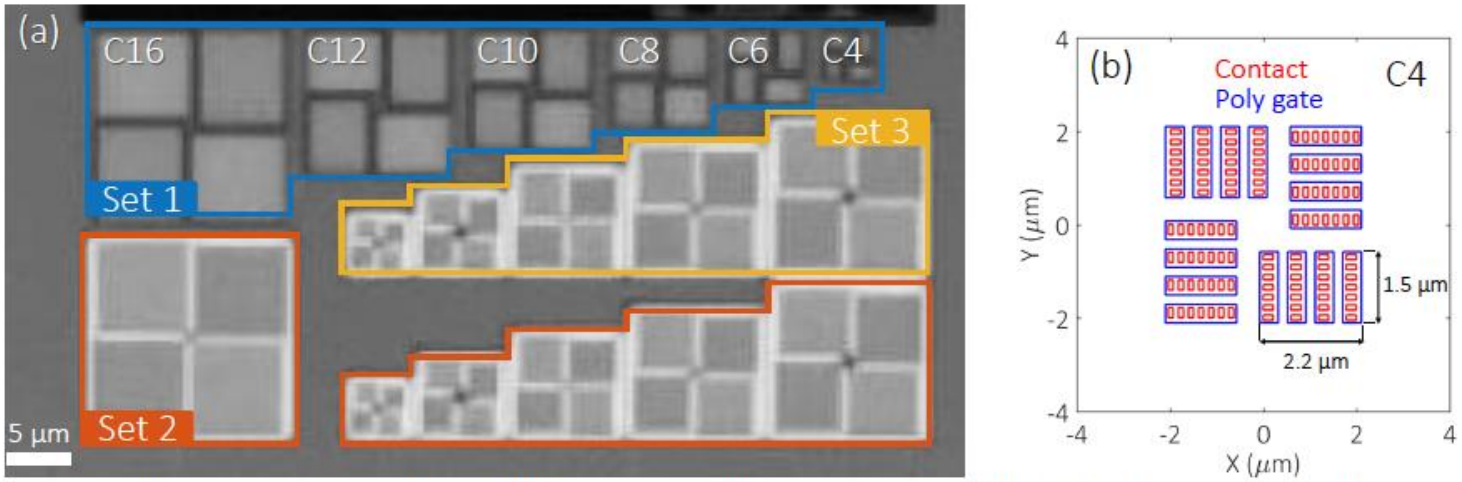


Figure 1. (a) Microscope image of the µDBO metrology block on a 28 nm FD-SOI production wafer. Three sets of six µDBO targets of varying size are printed in a contact - poly gate layer 64 times on the product reticle: 16×16 µm^2 (C16), 12×12 µm^2 (C12), 10×10 µm^2 (C10), 8×8 µm^2 (C8), 6×6 µm^2 (C6) and 4×4 µm^2 (C4). All targets sizes have three copies, indicated here by Set 1, 2 and 3. The C16 target of Set 3 is not shown, but located ~ 25 µm out of the imaged area. (b) The smallest target layout of C4 is shown for the two layers. The individual grating size is as small as 2.2 µm $\times$ 1.5 µm and consist of only four lines.

See also id. ("This is because we have added metrology tool-optical proximity correction (MT-OPC) assist features6 around the gratings. A separate study is dedicated to the impact of the MT-OPC and thus not in scope of this work. Smaller targets (< C10) are expected to have an affected overlay registration due to the following causes: At first targets below 10 x 10 µm2 have an individual grating size below 5 x 5 µm2 and should no longer be regarded as (pure) infinite gratings.7 Errors due to finite grating effects may emerge as a decreasing diffraction intensity (edge effects). This is because diffraction on such small targets occurs over a wider cone of angles and results in less diffracted photons captured by the optics."

Each of these maps includes one or more portions, depicted as different colored squares in the map. The squares represent the "the point-to-point difference in overlay." *Id.* at 2. The wafers being measured by the YieldStar system further includes "grating dimensions" which are "essential to select the right measurement recipe (wavelength and polarization) for an accurate overlay measurement. *Id.* at 4.

As a further example, the YieldStar system provides "customers with a high-density overlay map for every single TWINSCAN production wafer." *See* YieldStar 375F Product Overview, *available at* https://www.asml.com/en/products/metrology-and-inspection-systems/yieldstar-375f (last visited Oct. 12, 2020). As noted above, this mapping is performed on wafers with a grating

structure, and in multiple portions. See Overlay Study at 2-4.

See also Integrated ADI at Figs. 7 and 8:

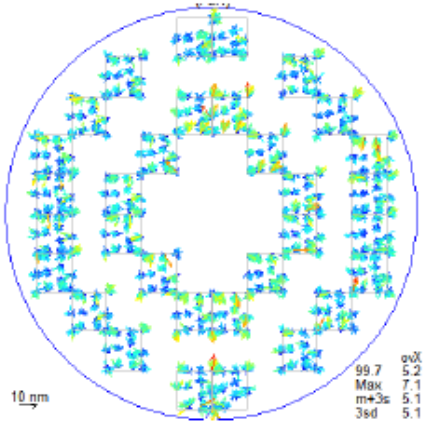


Figure 7: the sampling grid for the reference situation, and the residual OV using the typical APC correction model on this grid

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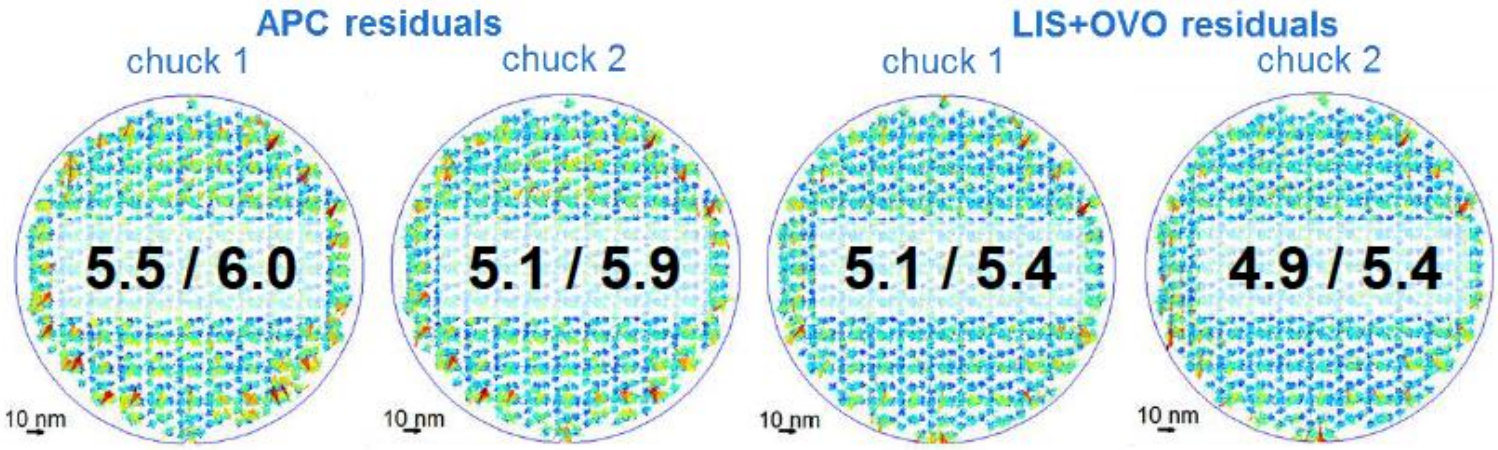
<td> 

Figure 8: the distribution and the m+3σ values of the simulated OV residuals, over 21 lots, 2 wfrs per lot, (left): for the reference situation, with a 416 points per wafer sampling grid, and typical correction model (right): for the integrated metrology situation, with 200 points per wafer sampling grid, LIS correction model</td>
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<td>concurrently measuring one or more critical dimensions and overlay in a wafer undergoing the fabrication process;</td>
<td>ASML’s YieldStar system concurrently measures one or more critical dimensions and overlay in a wafer undergoing the fabrication process;

For example, the YieldStar system measures multiple layers at the same time, wherein the layers consist of the critical dimension (“CD”) and an overlay during chip manufacturing, as follows:

“The YieldStar 1375F is the first YieldStar optical metrology system to offer measurements within the chip itself.

Capable of measuring multiple layers at once, this standalone system targets post-etch overlay and critical dimension (CD) measurements, allowing chipmakers to monitor the performance of their whole manufacturing process.”

See YieldStar 1375F Product Overview, available at https://www.asml.com/en/products/metrology-and-inspection-systems/yieldstar-1375f (last visited Oct. 12, 2020).

As an additional example, the YieldStar system measures CD and overlay in a single tool, as follows:

“The ASML YieldStar high NA angular resolved scatterometry system has the unique capability to measure overlay, scanner focus and critical dimension (CD) with one metrology tool. It offers the lithography engineer access to a wide variety of lithography</td>
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	parameters on overlay, focus and imaging profiles (CD, resist height, Side Wall Angle) as well as on the properties of the underlying stack (height, n, k).” *See* Integrated ADI at 1. *See also id.* at 3 (“3.3 CD monitoring Using the recipes described in the previous section, YieldStar CD measurements were collected over a 2 months period, covering more than 4000 wafers, 12 points per wafer, on the stand-alone tool, prior to install of the integrated tool. Note that during this period the recipes were not adapted. For a large part of these wafers also CD-SEM data was available on – pairwise – nearby locations on the wafer, on a target with slightly different nominal CD. The CD monitoring results for the L/S feature are shown in Figure 4. The raw data is split into mean per wafer and residuals, which was obtained after subtracting the mean per wafer and the average wafer fingerprint of the full data set. These residuals contain random effects such as tool repeatability, and the impact of local CD variations that are not averaged out by the sampling area of the measurement tool. It can be seen that the YieldStar residuals are almost 2 times smaller than those of the CD-SEM, in line with the better repeatability and the larger sampling area.”). *See also id.* at Fig. 4:

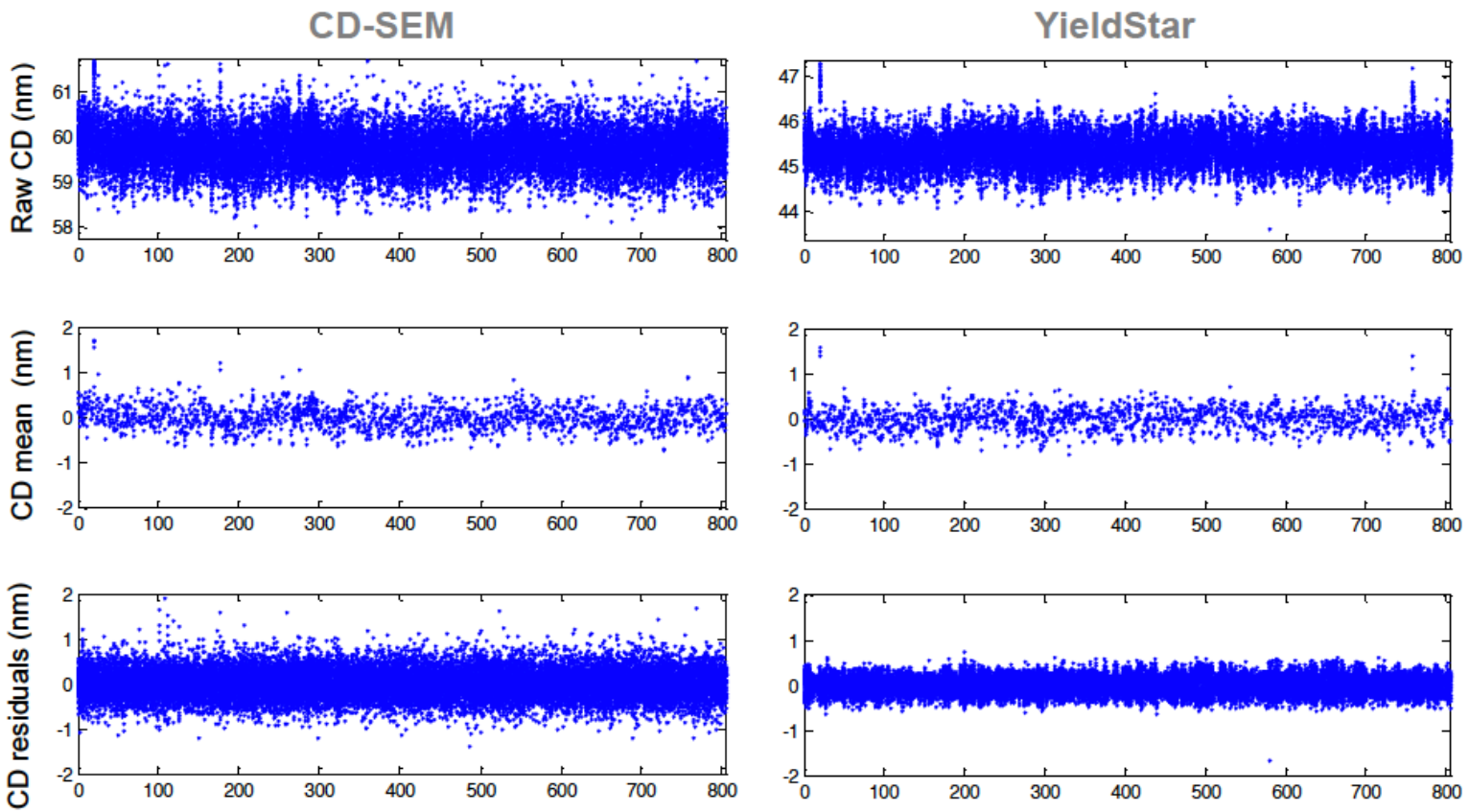
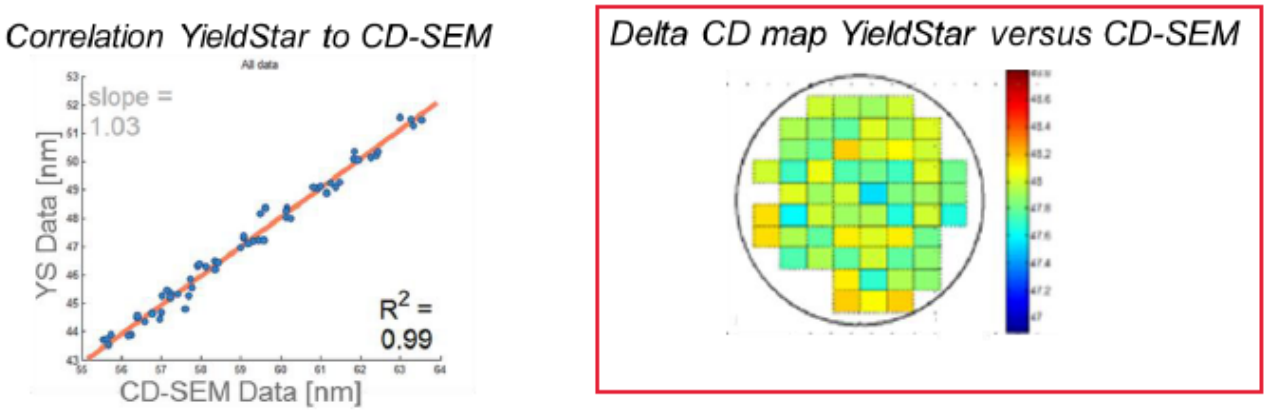
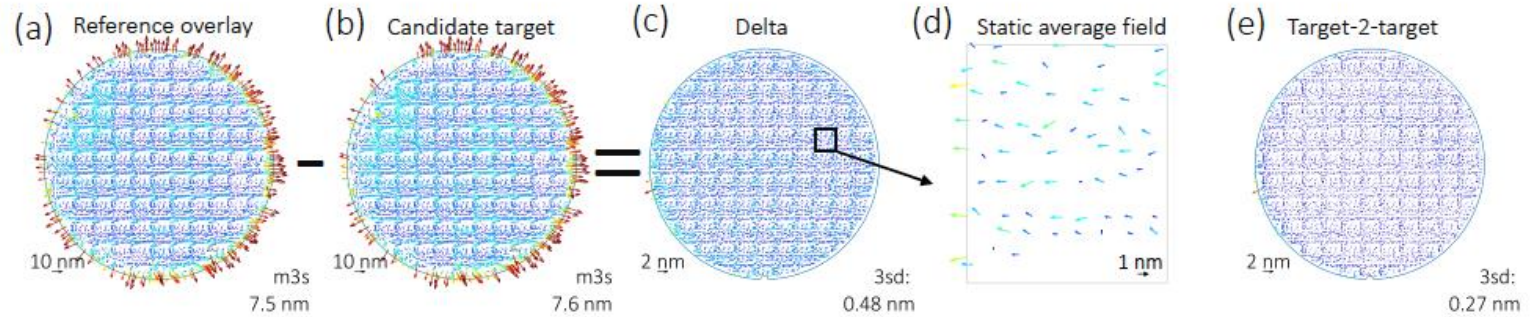


Figure 4: Monitoring data of CD [nm] of the L/S feature, measured by CD-SEM (left) and YieldStar (right); raw data (12 points per wafer) (top), variation of the mean-per-wafer (middle) and residuals after subtracting mean-per-wafer and average intra-wafer fingerprint (bottom)

See also id. at 4 ("From the mean-per-wafer plots, it can be seen that, irrespective of the CD metrology tool, the mean CD is well controlled within +/- 1nm, except for a few outliers. In addition to CD, the optical CD metrology tools can also measure many of the stack parameters. In Figure 5, as an example, the variation of the measured polysilicon height is shown. The data reveals that from lot 200 onwards, the polysilicon height follows a more or less bimodal distribution. Note that this variation didn't show up in the CD readings.")

See also id. at 5 ("As explained in the introduction, the YieldStar angular scatterometer can not only measure CD but also overlay (OV) and scanner Focus. The overlay measurement method used in the YieldStar is diffraction based overlay (DBO, see ref . [5] for more details).").

determining if one or more of the critical dimensions are outside of acceptable tolerances;	ASML's YieldStar system determines if one or more of the critical dimensions are outside of acceptable tolerances. For example, the YieldStar system generates a graph which shows the difference between wafer measurements and a metrology "recipe," as follows: Recipe creation for the CD measurements was aimed at obtaining recipes that have sufficient robustness against variations in height and optical properties of the layers in the underlying stack. Using a guided Recipe Creation Flow, supported by robustness simulations, it was determined which parameters in the feature model should remain fixed in the recipe and the overall best wavelength setting was selected. Figure 3 shows, for the final recipe for the L/S feature that the YieldStar measurements on a Focus-Exposure-Matrix (FEM) wafer match well, with an R^2 of 0.99, to those of the Tool-of-Record (CD-SEM). The measurements taken on a wafer printed at nominal Focus and Energy, a so-called CD-Uniformity (CDU) wafer, also shown in Figure 3, compared to CD-SEM, have a residual low frequency fingerprint below 0.5nm (3σ). The lack of a dominating systematic fingerprint in this delta CD wafer map is the first indication that the recipe is robust against cross-talk from variations in the underlying layers.  Figure 3: the correlation between YieldStar and ToR on a FEM wafer (left) and the difference between YieldStar and CD-SEM measurement on a CDU wafer (right) for the L/S feature of Figure 2. Note that the CD-SEM measurements on the FEM were taken on different targets with a different nominal CD than the YieldStar targets *See* Integrated ADI at 3. *See* Overlay Study at 3-4 ("We compare different sized targets with a reference overlay (Figure 2a). For the reference we have

	chosen the mean overlay of the three C16 targets per location. Next we take the point-to-point difference in overlay between the reference (Figure 2a) and the candidate (Figure 2b). As an example, we plot this difference in Figure 2c labelled "Delta". This "Delta" map is the difference overlay that can be broken down in the following contributors: 1. An overlay difference between the targets, that comes from reticle writing errors. This is systematic in the exposure eld. 2. Difference in interaction with the local environment between each target, leading to an overlay registration error (such as grating imbalance). Here it is assumed to be also systematic in the exposure eld. 3. Repeatability errors. These have a random nature. 4. Overlay registration error due to size di erence. We assume these to be both of random and systematic nature.”). *See also id.* at Fig. 2:  Figure 2. Dense overlay maps recorded on a YieldStar system. (a) The overlay map of the Reference overlay. The reference here is the mean overlay of the three C16 targets. (b) The reference overlay is compared to a candidate, here C16 Set 1. (c) The difference (”Delta”) between the reference and delta is shown, note the scale is now reduced to 2 nm. (d) The static average field is plotted and subsequently subtracted resulting in (e) the target-2-target delta map.
determining whether an overlay error is occurring;	ASML’s YieldStar system determines whether an overlay error is occurring. For example, where the YieldStar system identifies a delta, or difference, between the “recipe” and the recorded measurements, the system identifies those areas on the overlay map with a red color, as follows:

Recipe creation for the CD measurements was aimed at obtaining recipes that have sufficient robustness against variations in height and optical properties of the layers in the underlying stack. Using a guided Recipe Creation Flow, supported by robustness simulations, it was determined which parameters in the feature model should remain fixed in the recipe and the overall best wavelength setting was selected. Figure 3 shows, for the final recipe for the L/S feature that the YieldStar measurements on a Focus-Exposure-Matrix (FEM) wafer match well, with an R^2 of 0.99, to those of the Tool-of-Record (CD-SEM). The measurements taken on a wafer printed at nominal Focus and Energy, a so-called CD-Uniformity (CDU) wafer, also shown in Figure 3, compared to CD-SEM, have a residual low frequency fingerprint below 0.5nm (3σ). The lack of a dominating systematic fingerprint in this delta CD wafer map is the first indication that the recipe is robust against cross-talk from variations in the underlying layers.

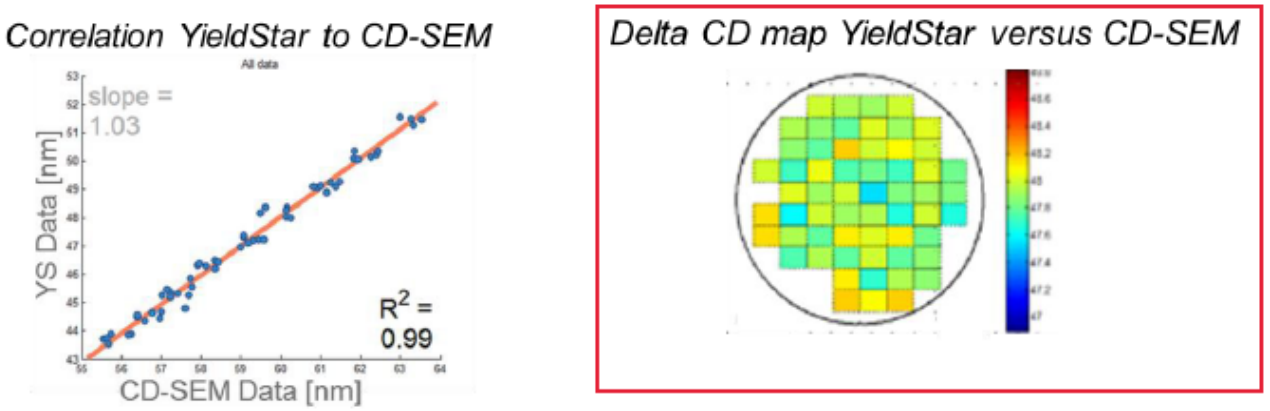


Figure 3: the correlation between YieldStar and ToR on a FEM wafer (left) and the difference between YieldStar and CD-SEM measurement on a CDU wafer (right) for the L/S feature of Figure 2. Note that the CD-SEM measurements on the FEM were taken on different targets with a different nominal CD than the YieldStar targets

See Integrated ADI at 3.

This red color represents a large variance from the "recipe."

See also id. at Figs. 7 and 8:

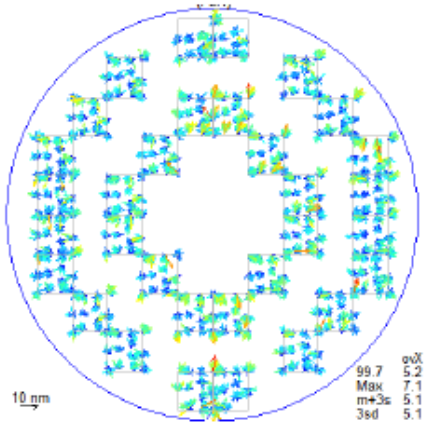


Figure 7: the sampling grid for the reference situation, and the residual OV using the typical APC correction model on this grid

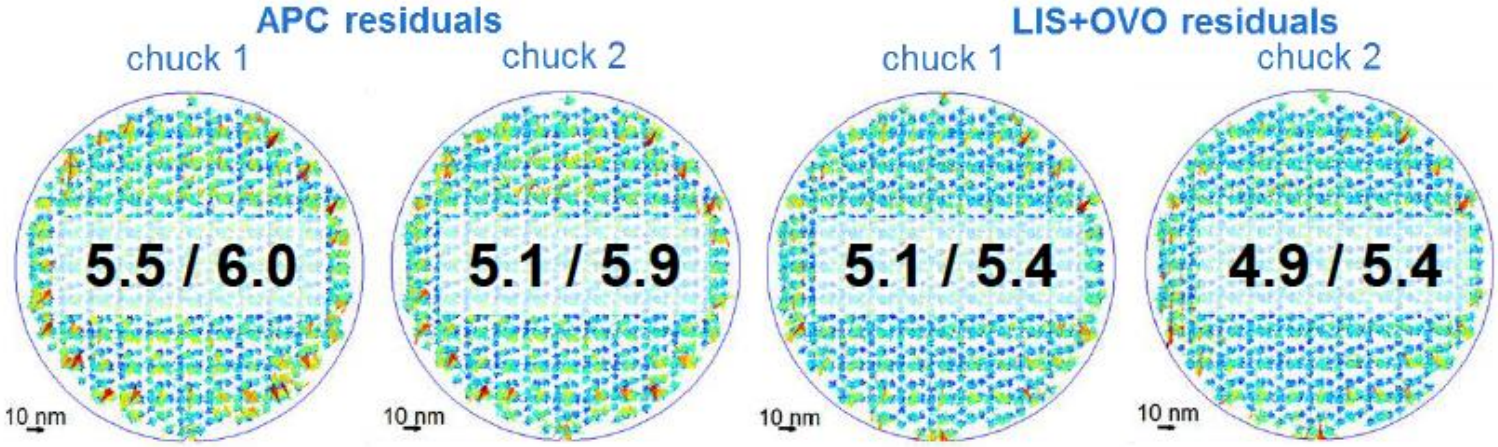
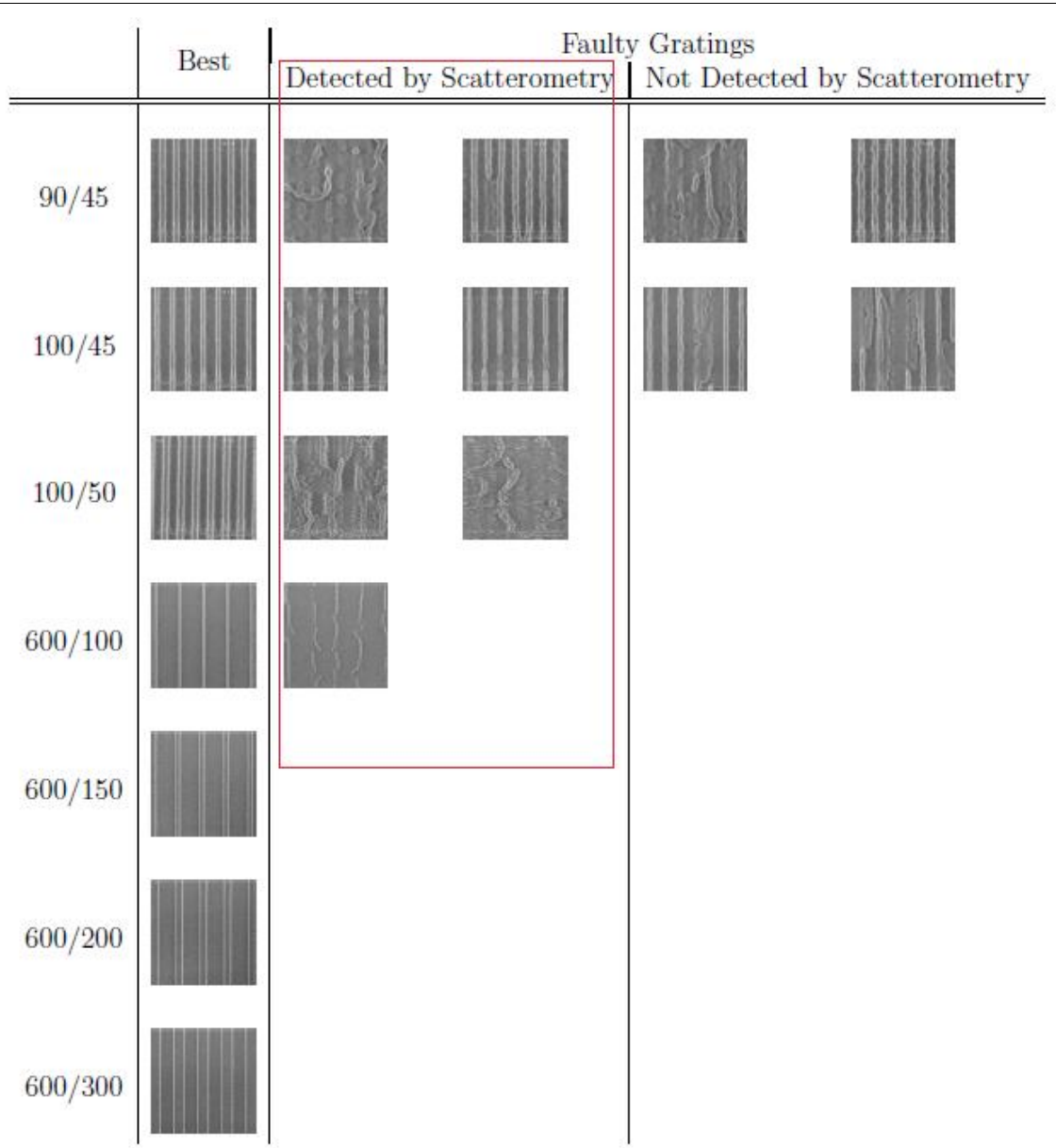


Figure 8: the distribution and the m+3σ values of the simulated OV residuals, over 21 lots, 2 wfrs per lot, *(left)*: for the reference situation, with a 416 points per wafer sampling grid, and typical correction model *(right)*: for the integrated metrology situation, with 200 points per wafer sampling grid, LIS correction model

Also, the YieldStar system flags "out-of-spec" measurements for further investigation, as follows. These "out-of-spec"

	measurements can include overlay errors: "Table 3.2: Sample images from FEM gratings. The first column shows the best focus and exposure for each grating. The second column shows faulty gratings that YieldStar flagged out-of-spec by outputting a small numeric measurement. The third column shows faulty gratings that YieldStar missed to flag. For context, there were 43 erroneous gratings judged from SEM images; YieldStar correctly flagged 39 samples."



See Jae Yeon Baek, Modeling and Selection for Real-time Wafer-to-Wafer Fault Detection Applications, *available at* http://www.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-215.html (last visited Oct. 12, 2020) ("Modeling and Selection").

See Overlay Study at 3-4 (“We compare different sized targets with a reference overlay (Figure 2a). For the reference we have chosen the mean overlay of the three C16 targets per location. Next we take the point-to-point difference in overlay between the reference (Figure 2a) and the candidate (Figure 2b). As an example, we plot this difference in Figure 2c labelled "Delta". This "Delta" map is the difference overlay that can be broken down in the following contributors: 1. An overlay difference between the targets, that comes from reticle writing errors. This is systematic in the exposure eld. 2. Difference in interaction with the local environment between each target, leading to an overlay registration error (such as grating imbalance). Here it is assumed to be also systematic in the exposure eld. 3. Repeatability errors. These have a random nature. 4. Overlay registration error due to size di erence. We assume these to be both of random and systematic nature.”).

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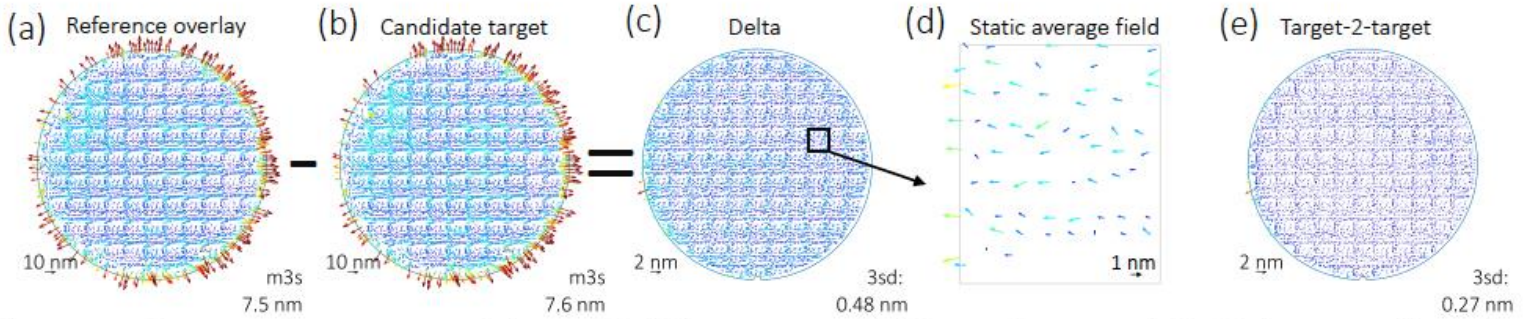

Figure 2. Dense overlay maps recorded on a YieldStar system. (a) The overlay map of the Reference overlay. The reference here is the mean overlay of the three C16 targets. (b) The reference overlay is compared to a candidate, here C16 Set 1. (c) The difference (”Delta”) between the reference and delta is shown, note the scale is now reduced to 2 nm. (d) The static average field is plotted and subsequently subtracted resulting in (e) the target-2-target delta map.

See also id. at 6 (“In Figure 4a we plot the C6 overlay as function of the reference C16 overlay. The C16 reference is the mean of the three C16 targets. We see a good point-to-point correlation, which is confirmed by a correlation coefficient of p = 0:99 and a linear t yields a slope here of 1:06.”)

See also id. at Fig. 4:

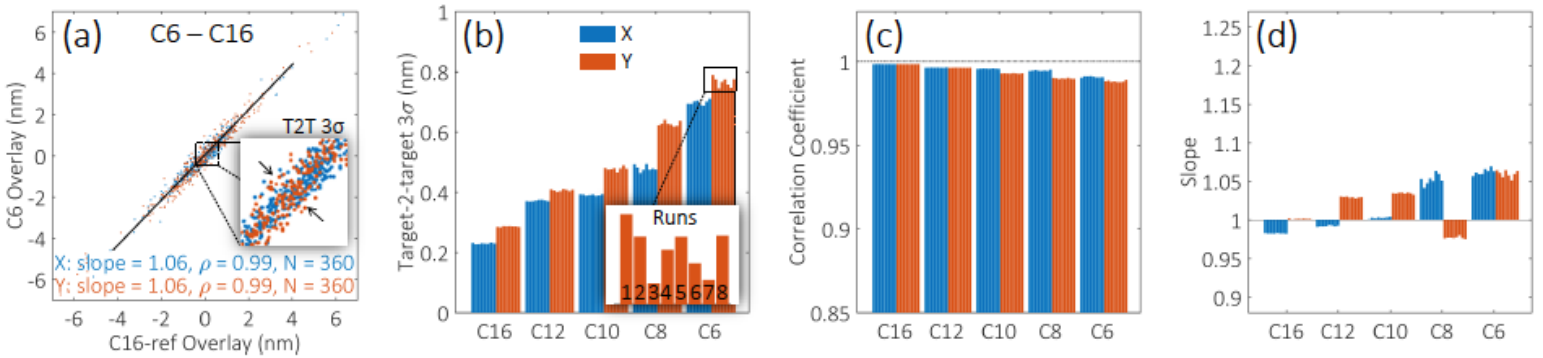

Figure 4. (a) The point-to-point plot of C6 overlay with C16 reference overlay is given for both directions x in blue and y in red. We find a very good correlation already with the smallest (C6 here) amongst the targets ($\rho = 0.99$). The inset zooms in on the spread of the data points. The spread is well described by the target-2-target 3σ variance, which is given in (b) for all targets and 8 runs for x and y. The inset in (b) zooms in on the target-2-target 3σ per run. Furthermore the correlation coefficient and slopes of all targets and 8 runs are shown in (c) and (d) respectively.

developing control data based upon one or more concurrent measurements when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances; and	ASML's YieldStar system develops control data based upon one or more concurrent measurements when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances. For example, the YieldStar system collects metrology data for the purpose of eventual control of the fabrication process, as follows: "Integrated metrology is aimed at optimal control of the production process by a enabling a combination of sufficiently dense sampling and a very short feedback time. However, during recipe preparation, and excursion diagnosis, the availability of a stand-alone tool that is matched to the integrated tool is pre-requisite. In the YieldStar platform this is accomplished by using the very same sensor design for both the integrated and the stand-alone configuration." *See* Integrated ADI at 6. This collected metrology data is then integrated into another tool for the purpose of process control. One such tool is ASML's LithoInsight correction model, as follows: "As explained in the introduction, the YieldStar angular scatterometer can not only measure CD but also overlay (OV) and scanner Focus. The overlay measurement method used in the YieldStar is diffraction based overlay (DBO, see ref .[5] for more details). This section deals with the OV sampling, correction models and the resulting control.

4.1 Overlay control using HVM sampling, LithoInsight model and Overlay Optimizer

To assess the overlay control capability offered by an integrated metrology solution, we compared a typical APC control case, as reference, with the integrated solution with optimized control model, sampling scheme and the full correction capabilities of the scanner.

* * *

"For the integrated solution, where the control is based upon metrology data from the integrated DBO tool, we used a LithoInsight (LIS) correction model."

See Integrated ADI at 5-6.

See also id. at Fig. 1:

Figure 1: the YieldStar metrology tool, integrated in the TEL track, can be used to generate the data necessary to improve overlay an d CD control

See also Modeling and Selection at 4 ("After the CD has been estimated for an incoming sample, R2R control algorithms are used to automate recipe corrections. One well-known algorithm is the exponentially weighted moving average (EWMA) filter."

feeding forward or backward the control data to adjust one or more fabrication components or one or more operating parameters associated with the fabrication components when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances to mitigate overlay error and/or to bring critical dimension within acceptable tolerances	ASML's YieldStar system feeds forward or backward the control data to adjust one or more fabrication components or one or more operating parameters associated with the fabrication components when at least one of an overlay error is occurring and one or more of the critical dimensions fall outside of acceptable tolerances to mitigate overlay error and/or to bring critical dimension within acceptable tolerances For example, the YieldStar system accomplishes metrology control by using the LithoInsight correction model, as follows: "In this paper, we have studied the wafer overlay correction capability by RegC® in combination with TWINSCANTM intra-field corrections to improve the on product overlay performance. RegC® is a reticle intra-volume laser writing technique that causes a predictable deformation element (RegC® deformation element) inside the quartz (Qz) material of a reticle. This technique enables to post-process an existing reticle to correct, for instance, for IPE. Alternatively, a pre-determined intra-field fingerprint can be added to the reticle such that it results in a straight field after exposure. This second application might be very powerful to correct for instance for (cold) lens fingerprints that cannot be corrected by the scanner itself. Another possible application is the intra-field processing fingerprint. One should realize that a RegC® treatment of a reticle generally results in global distortion of the reticle. This is not a problem as long as these global distortions can be corrected by the TWINSCANTM system (currently up to the third order). It is anticipated that the combination of the RegC® and the TWINSCANTM corrections act as complementary solutions. These solutions perfectly fit into the ASML LithoInsight product in which feedforward and feedback corrections based on YieldStar overlay measurements are used to improve the on product overlay." *See* Ofir Sharoni, Carl Zeiss, Intra-field on-product overlay improvement by application of RegC® and TWINSCANTM corrections, at 2, *available at* http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.682.133&rep=rep1&type=pdf (last visited Oct. 12, 2020). *See also id.* at Fig. 1:

Figure 1. Frame work in which the current work is positioned. Only the part marked in orange is addressed in this paper. It shows the co-optimization of the TWINSCAN™ and RegC® corrections within the Litho InSight (LIS) concept.

See also "Yieldstar S-1375F," *available at* https://www.asml.com/-/media/asml/files/products/yieldstar-systems/yieldstar-s-1375f.pdf ("By utilizing the YieldStar S-1375F's unique high-NA system, customers can measure device overlay and CD with speed and accuracy. This capability enables hyper dense sampling and faster feedback of after-etch data to the TWINSCAN and etchers.")

See also "Measuring accuracy," *available at* https://www.asml.com/en/technology/lithography-principles/measuring-accuracy (last visited Oct. 12, 2020) ("Additionally, YieldStar is being used for after-etch metrology to inspect actual device structures with more accuracy and higher measuring speed than our competitors' scanning electron microscope (SEM) solutions.").